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EXAMINER	
CAMPOS, YAIMA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,516	FLOMAN ET AL.	
	Examiner	Art Unit	
	YAIMA CAMPOS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/828,516, the examiner acknowledges the applicant's submission of the amendment dated March 12, 2008. At this point, claims 24, 41-42 and 45 have been amended and claims 1-23 stand canceled. Claims 24-46 are pending.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 24, 28-43 and 45-58** are rejected under 35 U.S.C. 103(a) as being unpatentable by Camacho et al. (US 6,167,487) in view of Ware et al. (US 6,826,657).

4. As per **claims 24, 41-42, 45 and 58**, Camacho discloses a memory unit comprising: "a first processor in communication with a memory unit, and a second processor in communication with the memory unit" " **["multi-port RAM that allows read and write accesses from different ports to be performed simultaneously" (Col. 1, lines 54-56)]** at least two memory areas **for** (*interpreted as intended use, see MPEP 2106 II-C*) storing data, **["a cache SRAM memory and a main DRAM memory arranged on the chip" (Col. 2, lines 10-19; Figure 1 and related text)]**

at least two memory areas for (interpreted as intended use, see MPEP 2106 II-C) storing data, **["a cache SRAM memory and a main DRAM memory arranged on the chip" (Col. 2, lines 10-19; Figure 1 and related text)]**

first terminals accessing data within the memory areas, second terminals for (interpreted as intended use, see MPEP 2106 II-C) accessing data within the memory areas, and **["single chip having first and second input/output pins" (Col. 2, lines 10-19; 28-45) "ports A and B" (Figure 1 and relate text)]**

at least two access controllers for (interpreted as intended use, see MPEP 2106 II-C) selectively providing **["the first data path may be controlled independently of the second data path" (Col. 2, lines 20-22) "port A control 22" and "port B control 24" (Figure 1 and related text)]**

sole addressing and accessing data through one of the terminals, and**["the first and second data path may be arranged so as to provide a single port for input/output of a data combination to or from the cache memory" (Col. 2, lines 46-52)]**

individual addressing and accessing data through each of the terminals, respectively, **["the first and second data paths may be arranged to provide input/output of data burst to or form the cache memory independently of each other" (Col. 2, lines 54-61)]**

wherein in case of sole addressing and accessing the data the access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of the terminals **["each of the ports A and B have address and control pins for receiving external address and control signals. The address and control signals for port A are independent from the address and control signals for port B" (Col. 5, lines 51-62) "data pins 18 and 20**

for supporting the output of the 16-bit data signals DQA and DQB for ports A and B" (Col. 6, lines 32-54) "A and B enables a user to combine them into a single 32-bit port. A unified-port mode of operation may be defined by a pre-set control signal supplied via an external pin... in the unified-port mode of operation, an external memory controller provides joint control of corresponding external control and address signals supplied to port A and port B control circuits 22 and 24 so as to perform a single 32-bit write or read access to the SRAM 16 via the both ports... further, if one port of the MPRAM 10 is disabled, the MPRAM 10 would be fully functional via the other port. In particular, any one of ports A and B enables read and write accesses to each and every location in the SRAM 16" (Col. 7, lines 33-56)].

Camacho does not disclose expressly wherein in the case of sole addressing, and data is provided within all of the at least two memory areas through data ports of both terminals.

Ware discloses a multi-port memory having two access modes (individual and sole) in which in case of sole addressing and accessing the data, the access controllers provide access to the memory areas by control ports and address ports of only one of the terminals and provides the data through data ports of both terminals as **[address ports A and data ports QDy and QDx wherein "first memory module 160 is connected to both the first port (Port 1a) 154 and the second port (Port 1b) 156 of the memory controller 152 through the QDx data bus and the QDy data bus" having half of the storage locations accessible through port 1a and half accessible through port 1b (Col. 15, line 47-Col. 16, line 13) "in the first memory module 160 are operated in the first mode with half of the storage location in the memory components (MEM) 174 accessible through the QDx data bus and the other half of the**

storage locations in the memory component (MEM) 174 accessible through the QDy data bus. It should be noted, however, that the memory components (MEM) 174 in the first memory module 160 may also be operated in the second mode with all of the storage locations accessible through the QDx data bus and the QDy data bus is unused" (Col. 15m lines 13-46) "FIG. 6B has the second memory module 172 connected to the third port (Port 2) 158 of the memory controller 152 through the QDx data bus. Thus, the memory components (MEM) 174 in the second memory module 172 are operated in the second mode with all of the storage locations accessible through the QDx data bus, and the QDy data bust is unused" (Figures 6A-6B and related text) "the type of access mode (i.e., either lockstep or independent) will depend upon both the source of a memory request (i.e, either the graphics processor or the main central processing unit) and/or the address of the memory request (lockstep region or independent region). The mode selection can be accomplished by a programmable register, fuse, jumper, etc. in the memory controller 352" (Col. 32, lines 16-23) (Col. 7, lines 6-25)]. Applicant should note that when accessing data through the QDx data bus, addresses and control signals are provided by A1a address bus while data is provided by data ports QDx1 and QxNs within port 1A (which are capable of accessing the entire memory 160 as chips 174 are all accessed by data ports QDx1 through QDxNs instead of providing access to half of the memory area through QDx and to the other half through QDy); which comprise two terminals. addresses and control signals are provided by A1a address bus while data is provided by data ports QDx1 and QxNs within port 1A (which are capable of accessing the entire memory 160 as chips 174 are all accessed by data ports QDx1 through QDxNs (*which comprises accessing the data through data ports of different terminals or both*

terminals), instead of providing access to half of the memory area through QDx and to the other half through QDy); which comprise two terminals, wherein the QDx data bus does not comprise a single data bus but multiple busses (QDx1 through QDxNs) accessing all of memory chips 174 in memory 160 (*thus providing "access to two memory areas by control and address ports of only one of the terminals and provide the data within all of the at least two memory areas through data ports of both terminals*).

Camacho et al. (US 6,167,487) and Ware et al. (US 6,826,657) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory unit as disclosed by Camacho and further provide of sole addressing and accessing the data the access controllers provide access to the memory areas by control ports and address ports of only one of the terminals and provides the data through data ports of both terminals as disclosed by Ware.

The motivation for doing so would have been because Ware discloses sole addressing and accessing the data the access controllers provide access to the memory areas by control ports and address ports of only one of the terminals and provides the data through data ports of both terminals is done as [**"These solutions provide maximum memory bandwidth across the full memory address space when the memory system is constrained to a single memory module per memory controller port, and the memory modules are allowed to have different densities and organizations. These solutions also keep memory bandwidth (and other performance metrics) as balanced as possible across the entire memory space" (Col. 32, line 66-Col. 33, line 6)**].

Therefore, it would have been obvious to combine Camacho et al. (US 6,167,487) with Ware et al. (US 6,826,657) for the benefit of creating a memory unit to obtain the invention as specified in claims 24, 41-42 and 45.

5. As per **claim 28**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein the first and/or second terminal comprises control ports for (interpreted as intended use, see MPEP 2106 II-C) receiving control signals for (interpreted as intended use, see MPEP 2106 II-C) controlling access to the memory areas **["each of the ports A and B have address and control pins for receiving external address and control signals. The address and control signals for port A are independent from the address and control signals for port B;" control ports "SCA" and "SCB" (Col. 5, lines 51-62; Figure 1 and related text)]**.

6. As per **claim 29**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein the first and/or second terminal comprises address ports for (interpreted as intended use, see MPEP 2106 II-C) receiving addressing signals for (interpreted as intended use, see MPEP 2106 II-C) addressing data within the memory areas **["each of the ports A and B have address and control pins for receiving external address and control signals. The address and control signals for port A are independent from the address and control signals for port B;" address ports "ADA" and "ADB" (Col. 5, lines 51-62; Figure 1 and related text)]**.

7. As per **claim 30**, the combination of Camacho and Ware discloses the memory unit of claim 29, wherein the address ports provide access to an external address bus **["each of the ports A and B have address and control pins for receiving external address and control**

signals. The address and control signals for port A are independent from the address and control signals for port B" (Col. 5, lines 51-62; Figure 1 and related text)].

8. As per **claim 31**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein the first and/or second terminal comprises data ports for (interpreted as intended use, see MPEP 2106 II-C) reading and/or writing data to and/or from the memory areas **["data pins 18 and 20 for supporting the output of the 16-bit data signals DQA and DQB for ports A and B" (Col. 6, lines 32-54; Figure 1 and related text)]**.

9. A per **claims 32-33**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein the access controllers provide access to the data areas based on control and/or address signals at said terminals wherein the access controllers are state machines, the state machines providing access to the data areas based on states of signals at the first and second terminals. **["SRAM control signals SCA and SCB for the ports A and B, respectively, are supplied via a port A control circuit 22 and a port B control circuit 24 to define SRAM operations such as data read or write, and burst termination" (Col. 3, lines 47-56) "each of the ports A and B comprises a pipelined data path having pipeline stage 1 and pipeline stage 2. The pipeline stages 1 include decoding circuits 110A and 110B, address latches 112A and 112B, and main amplifiers 114A and 114B for ports A and B, respectively… a deselect signal may be supplied to each of the decoding circuits 110A and 110B to inhibit the ports from accepting commands. For example, the deselect signal may be produced when the chip select signal /SS is set to a predetermined state" (Col. 6, lines 15-41; Figure 4 and related text)]**.

10. As per **claim 34**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein the access controllers comprise memory registers **["write per bit mask registers 34 and 36" (Col. 4, lines 34-51) "data transfer registers 44" (Col. 5, lines 6-21) "mode register" (Col. 5, lines 22-37)]**.

11. As per **claims 35-36**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein the access controllers provide access to at least one memory area by the control ports and the address ports of the terminals, respectively, and provides the data through the data ports of the terminals, respectively, in case of individual addressing wherein the access controllers provide access to at least one memory area by both of the control ports and the address ports of the terminals, and provide the data through the data ports of the terminals, respectively, in case of individual addressing **["a set mode register command SMR issued by the DRAM control circuit 42 enables the burst length and type to be programmed in an internal mode register. Ports A and B may be programmed individually so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data burst of another length… one port may be programmed to support sequential addressing of data bursts, whereas the other port may be programmed to provide interleave addressing… each port has its own independent burst length counter, burst termination logic and memory addressing logic. Therefore, the burst mode operations for port A may be carried out independently of burst mode operations for port B" (Col. 7, line 57-Col. 8, line 31)]**.

12. As per **claim 37**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein at least two memory areas are provided **["a cache SRAM memory and a**

main DRAM memory arranged on the chip" (Col. 2, lines 10-19; Figure 1 and related text)].

13. As per **claim 38**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein programming the size of the memory areas is provided through one of the terminals **["each port has its own independent burst length counter, burst termination logic and memory addressing logic. Therefore, the burst mode operations for port A may be carried out independently of burst mode operations for port B" (Col. 8, lines 27-31)]**.

14. As per **claim 39**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein one of the terminals provides accessing the data by a central processing unit, and wherein one of the terminals provides accessing the data by a graphics processor **["a multi-port RAM that allows read and write accesses from different ports to be performed simultaneously" (Col. 1, lines 65-67; Col. 1, lines 13-60)]**.

15. As per **claim 40**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein the bandwidth and/or clocking frequency for (interpreted as intended use, see MPEP 2106 II-C) the terminals is different **["Ports A and B may be programmed individually so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data burst of another length" (Col. 7, line 57-Col. 8, line 31)]**.

16. As per **claim 43**, the combination of Camacho and Ware discloses a module for (interpreted as intended use, see MPEP 2106 II-C) providing memory to processors, comprising connection terminals providing communication between an electronic circuit and a memory unit according to claim 24 **[busses (Figure 1 and related text)]**.

17. As per **claims 25 and 47**, the combination of Camacho and Ware discloses the memory unit of claim 24, wherein a memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals, respectively [**"a set mode register command SMR issued by the DRAM control circuit 42 enables the burst length and type to be programmed in an internal mode register. Ports A and B may be programmed individually so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data burst of another length… one port may be programmed to support sequential addressing of data bursts, whereas the other port may be programmed to provide interleave addressing… each port has its own independent burst length counter, burst termination logic and memory addressing logic. Therefore, the burst mode operations for port A may be carried out independently of burst mode operations for port B" (Col. 7, line 57-Col. 8, line 31)**] wherein a third memory area a memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals [**Ware discloses this limitation (Figure 13C and related text)**].

18. As per **claims 26 and 48** , the combination of Camacho and Ware discloses the memory unit of claim 25, wherein two of the three memory areas provide access by the control ports and the address ports of the terminals, respectively, and the data through the data ports of the terminals, respectively [**The same rationale in the rejection to claims 35-36 is herein incorporated**].

19. As per **claims 27 and 49**, the combination of Camacho and Ware discloses the memory unit of claim 25, wherein the access controllers provide prioritized access to the third memory

area through one of the terminals **[Camacho discloses this limitation as "chip select signals /SD and /SS provide chip select functions for the DRAM 12 and the SRAM 16, respectively" (Col. 3, lines 62-64) wherein "if one port of the MRAM 10 is disabled, the MRAM 10 would be fully functional via the other port. In particular, any one of ports A and B enables read and write accesses to each and every location in the SRAM 16" (Col. 7, lines 52-56) Ware discloses this limitation (Col. 15, line 13-Col. 16, line 13)]**.

20. As per **claims 46 and 50**, the combination of Camacho and Ware discloses the memory unit of claim 45, wherein a memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals, respectively **["a set mode register command SMR issued by the DRAM control circuit 42 enables the burst length and type to be programmed in an internal mode register. Ports A and B may be programmed individually so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data burst of another length… one port may be programmed to support sequential addressing of data bursts, whereas the other port may be programmed to provide interleave addressing… each port has its own independent burst length counter, burst termination logic and memory addressing logic. Therefore, the burst mode operations for port A may be carried out independently of burst mode operations for port B" (Col. 7, line 57-Col. 8, line 31)]** three memory areas in a memory unit wherein a third memory area a memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals, respectively as **[Ware discloses this limitation (Figure 13C and related text)]**.

21. As per claim 51, the combination of Camacho and Ware discloses The method of claim 41, wherein addressing signals for addressing data within the memory areas are received by address ports of the first and/or second terminal **[Ware discloses addressing signals are received by A1a and A1b (fig. 6B and related text)]**.

22. As per claim 52, the combination of Camacho and Ware discloses The method of claim 51, wherein an external address bus is accessed by the address ports provided **[Ware discloses addressing signals are received by A1a and A1b (fig. 6B and related text)]**.

23. As per claim 53, the combination of Camacho and Ware discloses The method of claim 41, wherein data to and/or from the memory areas is read and/or written by data ports of the first and/or second terminal **[Ware discloses data ports QD1-QDNs in 1a and 1b (fig. 6B and related text)]**.

24. As per claim 54, the combination of Camacho and Ware discloses The method of claim 41, wherein the access controllers access the data areas based on control and/or address signals at said first and second terminals **[Ware discloses addressing signals are received by A1a and A1b (fig. 6B and related text)]**.

25. As per claim 55, the combination of Camacho and Ware discloses The method of claim 41, wherein the access controllers are state machines, the state machines accessing the data areas based on states of signals at the first and second terminals **[Ware discloses addressing signals are received by A1a and A1b (fig. 6B and related text)]**.

26. As per claim 56, the combination of Camacho and Ware discloses The method of claim 41, wherein the access controllers accesses at least one memory area by the control ports and the address ports of the terminals, respectively, and provide the data through the data ports of the

terminals, respectively, in case of individual addressing **[The rationale in the rejection to claim 41 is herein incorporated. Ware teaches accessing data through address terminals A1a and A1b and data terminals QD1-QDNs in 1a and QD1-QDNs in 1b]**.

27. As per claim 57, the combination of Camacho and Ware discloses The method of claim 56, wherein the access controllers access at least one memory area by both of the control ports and the address ports of the terminals, and provide the data through the data ports of the terminals, respectively, in case of individual addressing **[The rationale in the rejection to claim 41 is herein incorporated. Ware teaches accessing data through address terminals A1a and A1b and data terminals QD1-QDNs in 1a and QD1-QDNs in 1b]**.

28. **Claim 44** is rejected under 35 U.S.C. 103(a) as being unpatentable over Camacho et al. (US 6,167,487) and Ware et al. (US 6,826,657) as applied to claim 24 above and further in view of below

29. It is noted that the combination of Camacho and Ware does not disclose a mobile communication device comprising a memory unit according to claim 24. However, the examiner asserts that it would have been obvious to one ordinary skill in the art at the time the invention was made to use the memory as being claimed in claim 24 in a mobile communication device. A recitation directed to the manner in which a claim is intended to be used does not distinguish the claim from the prior art if prior art has the capability to do so (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987).

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

30. Applicant's arguments filed September 2, 2008 have been fully but they are not persuasive.

31. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

32. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

FIRST POINT OF ARGUMENT

33. Regarding Applicant's remark that the combination of Camacho and Ware does not disclose sole addressing and accessing the data, where access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of the terminals and provide the data within both of the two memory areas through data ports of both terminals is not disclosed by Ware; this argument has been fully considered but it is not deemed persuasive.

34. More specifically, Applicant argues "Ware, within which all of the storage locations are accessible through the QDx data bus, while the QDy data bus is unused. By providing access through all storage locations through only one data bus, different to the teaching of the invention wherein all of the at least two memory areas are accessed through data ports of both terminals, the data bandwidth cannot be increased according to the Ware teaching" (page 9 of Applicant's remarks filed on March 12, 2008).

This argument has been fully considered but it is not deemed persuasive as it appears that Applicant is mischaracterizing Examiner's rejection as Applicant should note that when

accessing data through the QDx data bus, addresses and control signals are provided by A1a address bus while data is provided by data ports QDx1 and QxNs within port 1A (which are capable of accessing the entire memory 160 as chips 174 are all accessed by data ports QDx1 through QDxNs (*which comprises accessing the data through data ports of different terminals or both terminals*), instead of providing access to half of the memory area through QDx and to the other half through QDy); which comprise two terminals, wherein the QDx data bus does not comprise a single data bus but multiple busses (QDx1 through QDxNs) in 1a accessing all of memory chips 174 in memory 160 (*thus providing "access to two memory areas by control and address ports of only one of the terminals and provide the data within all of the at least two memory areas through data ports of both terminals*).; thereby providing maximum bandwidth. Ware specifically discloses **["FIG. 6B has the second memory module 172 connected to the third port (Port 2) 158 of the memory controller 152 through the QDx data bus. Thus, the memory components (MEM) 174 in the second memory module 172 are operated in the second mode with all of the storage locations accessible through the QDx data bus, and the QDy data bust is unused" (Figures 6A-6B and related text) "the type of access mode (i.e., either lockstep or independent) will depend upon both the source of a memory request (i.e, either the graphics processor or the main central processing unit) and/or the address of the memory request (lockstep region or independent region)" (Col. 32, lines 16-23) (Col. 7, lines 6-25) (Refer to Figure 6B and related text) and explains** as **"These solutions provide maximum memory bandwidth across the full memory address space when the memory system is constrained to a single memory module per memory controller port, and the memory modules are allowed to have different densities and organizations. These solutions**

also keep memory bandwidth (and other performance metrics) as balanced as possible across the entire memory space" (Col. 32, line 66-Col. 33, line 6)].

Applicant should note that the pending claims do not further define the terms "terminals" or "data ports" to preclude QD1-QDN in Port 1a ports in Ware from reading on data ports of different terminals as claimed.

35. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated September 2, 2008.

36. **CLOSING COMMENTS**

Examiner's Note

37. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

38. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

39. Per the instant office action, claims 24-58 have received an action on the merits and are subject of a final rejection.

a(2) CLAIMS NO LONGER UNDER CONSIDERATION

40. Claims 1-23 stand cancelled as of amendment received on September 2, 2008.

b. DIRECTION OF FUTURE CORRESPONDENCES

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

42. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions

on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 8, 2008

/Yaima Campos/
Examiner, Art Unit 2185

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185